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Analysis of cascaded H-bridge multilevel inverter configuration with double level circuit

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Abstract: In this study, a new multilevel inverter configuration which introduces a combination of cascaded H-bridge multilevel inverter with a double level circuit is proposed. The double level circuit is a half-bridge inverter when combined with a cascaded H-bridge multilevel inverter, will increase the output voltage level to nearly twice that of a conventional cascaded H-bridge multilevel inverter. The effectiveness of the proposed configuration is demonstrated with five different cases of cascaded H-bridge multilevel inverter configurations. Phase disposition carriers arrangement with sinusoidal reference has been utilised in pulse width modulation for generating the gating signal of switches to achieve high-quality output voltage waveform. A comparison is carried out with different parameters such as %total harmonic distortion, distortion factor, the maximum voltage step of output voltage level and peak inverse voltage. Analysis of power loss and theoretical calculation of %total harmonic distortion is described. Also, a new method for calculating the overall component count is discussed. As a result, the proposed configuration requires lesser component count for generating higher output voltage level with lower %total harmonic distortion. Selected simulation and experimental results are shown to verify and validate the proposed multilevel inverter configuration.

Nomenclature

V_o	output voltage of H-bridge in V
V_{HBK}	kth bridge output voltage ($k = 1$ to N) in V
$V_{dc,j}$	DC source voltage ($j = 1$ to N) in V
V_{dcx}	DC source voltage of DLC circuit in V
C_1–C_{14}	Boolean output from sinusoidal pulse width modulation in V
P_{cl}	conduction loss in W
P_{sl}	switching loss in W
P_l	total power loss in W
$P_{cl,k}$	total conduction loss of kth switch in W
$P_{sl,k}$	total switching loss of kth switch in W
$E_{on,k}$	energy loss during turn-on time of kth switch in mJ
$E_{off,k}$	energy loss during turn-off time of kth switch in mJ
I and I'	current in A
f	frequency in Hz
t_{on}	turn-on time in ns
t_{off}	turn-off time in ns
$v_{sw,k}$	off-state voltage of the kth switch in V
$P_{cl,t,k}$	conduction losses of kth switch in W
$P_{cl,d,k}$	conduction losses in kth anti-parallel diode in W
V_t	on-state voltage of switch in V
V_d	on-state voltage of diode in V
r_t	collector emitter on-state resistance of switch in Ω
r_d	collector emitter on-state resistance of diode in Ω
$I_{t,avg}$	average switch current in mA
$I_{t,rms}$	root-mean-square (RMS) switch current in mA
$I_{d,avg}$	average switch current in mA
$I_{d,rms}$	RMS switch current in mA
S_1–S_{14}	insulated-gate bipolar transistor switches
N_S	number of switches
N_C	number of capacitors
N_D	number of diodes
N_{DC}	number of DC source
N_T	number of transformers
N_X	number of other components
N_P	number of poles
F_L	per level factor

1 Introduction

Multilevel inverter (MLI) normally integrates the step voltage waveform from several levels of DC voltage sources. The MLI is utilised for reducing the harmonic distortion, electromagnetic interference problems and also the high-frequency switching dv/dt induced motor failures [1]. Additionally, as the number of steps increases in the output voltage waveform, the harmonic distortion of waveform decreases and also reduces the size of required passive filters [2]. Hence, MLIs are widely employed in high-power applications that incorporate renewable energy, conveyors, blowers, laminators and so on. The detailed principles of three conventional MLI configurations are presented to generate staircase output voltage waveform, i.e. neutral point clamped MLI (NPCMLI) or diode clamped MLI (DCMLI), flying capacitor MLI (FCMLI) and cascaded H-bridge MLI (CHBMLI) [3]. The drawbacks of DCMLI configuration are the unequal loss distribution among the semiconductors and unequal temperature distribution. Also, a new active NPCMLI (ANPCMLI) configuration is reported [4] to overcome the problem of DCMLI. Both ANPCMLI and DCMLI require more clamping diodes and FCMLI requires more clamping capacitors. Therefore, the circuit becomes bulky and complex to design. One of the significant constraints in DCMLI and FCMLI is the voltage unbalance in DC link capacitors which causes unbalance in output voltage level [5]. Single-phase full-bridge inverter with separate DC source is connected in series and it acts as CHBMLI. It has some of the focal points when compared with other conventional MLI configuration. Clamping diodes and clamping capacitors are not required and also it needs a separate DC source for each and every H-bridge unit. Therefore, it is simpler to integrate with renewable energy sources such as solar, fuel cells and biomass but depending on rating of the DC source [6, 7]. Conventional MLIs are utilised in renewable energy application [8] also in FACTS devices [9–11].

Numerous researchers are endeavouring to develop a new configuration of MLI or to re-modify the existing ones for improving the quality of waveforms and to reduce the count of switches, driver circuits and DC sources. Different types of MLI

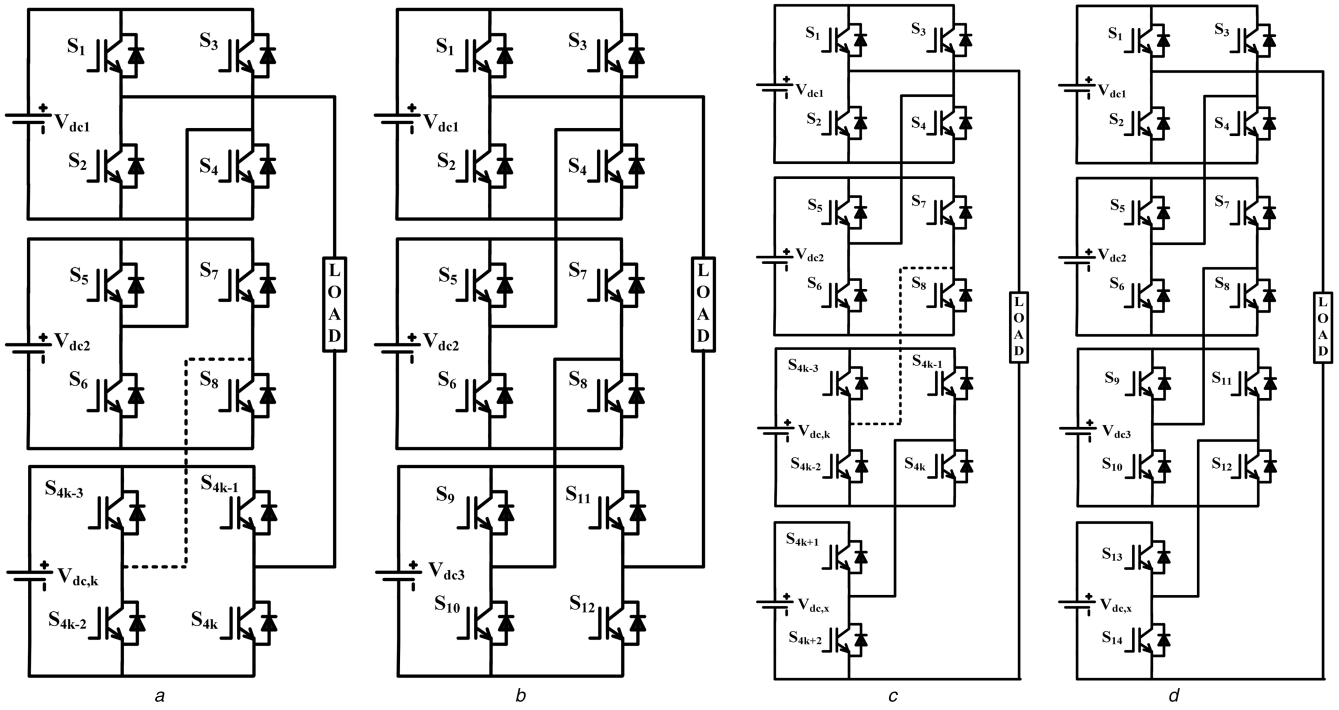

Fig. 1 *Proposed topology of MLI*

(a) Generalised CHBMLI, ***(b)*** CHBMLI configuration with three DC sources, ***(c)*** Generalised proposed MLI configurations, ***(d)*** Proposed MLI configuration with three CHBMLIs

configuration are presented in [12–16]. These configurations are not well equipped for getting all the combination of addition and subtraction of the input DC sources to generate the output waveform without any modification in the basic unit. Therefore, to overcome this issue, the basic unit is connected in series to achieve the required output voltage level. However, the component count (DC source and switches) utilised in these topologies will increase when compared with the conventional CHBMLI. Single DC source with floating MLI or FCMLI is developed [17–20] for reducing the DC source count. The developed configuration utilises bidirectional switches and floating capacitors which makes the circuit complex and increases the switch count [19]. Extra control circuits are needed for balancing the capacitor voltage [20]. On the other hand, a single-phase transformer/three-phase transformer based CHBMLI is developed. In this case, primary of each transformer is connected to cascaded H-bridge (CHB) output side and secondary is connected in series to achieve the desired voltage level [21]. The disadvantage of this configuration is while deciding turns ratio of the transformer where its size increases due to increase in output voltage level. Hybrid topologies are also recently developed for making the quality of output voltage waveform in [22–24] which require higher number of different voltage magnitude DC sources. Generally, asymmetric DC source MLI generates higher output voltage steps with lower %total harmonic distortion (%THD) compared with symmetric MLI. The different types of asymmetric algorithm are reported [13, 17] for fixing the DC source magnitude value and generating higher number of levels. However, increasing cost is the main drawback of asymmetric DC sources. Frequency is one of the major aspects for generating quality output voltage waveform in MLI. Generally, good quality waveform is generated by higher switching frequency when compared with lower switching frequency. Also, higher switching frequency waveform requires lesser filter size while interconnecting to the grid system. Therefore, higher switching frequency is chosen for generating the switching pulses to the proposed MLI topology.

In this paper, a unique method of choosing DC source magnitude for the double level circuit (DLC) and integrating it appropriately in the CHBMLI circuit to overcome the above-mentioned drawbacks is proposed. The value of DC source in the DLC circuit is only half the value of first H-bridge inverter. The main advantage of this selection of DC source is the utilisation of low-voltage magnitude DC source for increasing output voltage steps. The usage of DLC circuit increases the output voltage level to nearly twice that of conventional CHBMLI output voltage level without affecting the maximum output voltage steps. Also, this paper deals with five different combinations of DC source ratio for MLI configuration with and without DLC circuit. These combinations show the capability of the configuration to generate five different levels of output voltage using the same proposed configuration by changing the connected DC sources. Theoretical calculation of %THD using asymptotic formula is discussed with suitable equation. A new method of calculating the total device count is presented in Section 5. Calculation of power losses with appropriate equations is discussed. To conclude, the proposed MLI configuration is identified to require lesser number of device counts for the desired output voltage level. The proposed MLI configuration has been validated with experimental and simulation results. The proposed MLI topology has some advantages when compared with other topologies such as reduced number of switches for generating higher number of output voltage level, lesser %THD, lesser switching losses and conducting losses. The proposed MLI topology is a convenient solution for photovoltaic application. Separate DC sources can be replaced by separate photovoltaic panels with appropriate boost converter and maximum power point technique. As a continuation, the proposed MLI topology would be tested for photovoltaic application in future.

2 CHB multilevel inverter

A generalised CHBMLI is demonstrated using series connected single-phase full-bridge inverter with separate DC source [4, 6]. The purpose of series connection is to the increase number of levels in output voltage and also to reduce the harmonic distortions in it [5]. The generalised configuration of CHBMLI is displayed in Fig. 1*a*, which consists of k-full-bridge inverters with separate DC source. The output voltage waveform is generated by adding each H-bridge output voltages together

$$V_{\mathrm{o}} = \sum_{k=1}^{N} V_{\mathrm{HB}k} = V_{\mathrm{HB1}} + V_{\mathrm{HB2}} + V_{\mathrm{HB3}} + \cdots + V_{\mathrm{HB}N} \tag{1}$$

Here, V_{o} represents the output voltage of CHBMLI and $V_{\mathrm{HB}k}$ represents kth H-bridge output voltage. Symmetric and asymmetric conditions are the major classification of MLI based on DC source.

In this paper, the conventional CHBMLI (symmetric MLI) and four types of asymmetric MLI configuration are discussed, such as natural sequence MLI, binary MLI, quasi-linear MLI and trinary MLI. In addition, the above-mentioned types of CHBMLI are tested with the proposed DLC to enhance the quality of output voltage waveform and also to reduce the %THD.

3 Proposed multilevel inverter configuration

Even though the configuration of CHBMLI with half-bridge inverter has already been introduced in [25, 26], the concept of DLC has not been utilised. Whereas the proposed MLI configuration is a combination of k-full-bridge inverter (CHB inverter) in series with a half-bridge inverter as shown in Fig. 1*c*. The single half-bridge inverter integrated with the circuit acts as a DLC in this configuration. The main aim of DLC is to increase the output voltage level to nearly twice that of the conventional CHBMLI output voltage level, while simultaneously reducing the number of switches and its voltage rating. To avoid short circuit, switches of the half-bridge are not turned-on simultaneously. When the DLC circuit is connected to CHBMLI, odd levels are produced in output voltage levels of each half-cycle. When the DLC circuit is disconnected from CHBMLI, the output voltage will have only even levels in each half-cycle. Subsequently by joining both voltage levels, the desired output voltage level is produced in the proposed MLI configuration. The DC source value of DLC circuit is half the value of first entity of DC source in CHBMLI. The output voltage of CHBMLI with DLC cannot be symmetrical because levels of positive cycle will be more than that of negative cycle. Therefore, to make the output voltage waveform symmetrical, appropriate logic is designed as in Section 4. Table 1 shows all the switching combinations for positive half-cycle of generalised proposed MLI. The number of switches used in CHBMLI with and without DLC is given below

Table 1 Switching table for positive half-cycle of generalised proposed MLI configuration

Sl. no.	Possible combination of output voltage (V_o)	On-state switches
1	V_{dcx}	S_2, S_4, S_6, S_8, S_{4k-2}, S_{4k}, S_{4k+1}
2	V_{dc1}	S_1, S_4, S_6, S_8, S_{4k-2}, S_{4k}, S_{4k+2}
3	$V_{dc1} + V_{dcx}$	S_1, S_4, S_6, S_8, S_{4k-2}, S_{4k}, S_{4k+1}
4	$V_{dc2} - V_{dc1}$	S_2, S_3, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+2}
5	$V_{dc2} - V_{dc1} + V_{dcx}$	S_2, S_3, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+1}
6	V_{dc2}	S_2, S_4, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+2}
7	$V_{dc2} + V_{dcx}$	S_2, S_4, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+1}
8	$V_{dc1} + V_{dc2}$	S_1, S_4, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+2}
9	$V_{dc1} + V_{dc2} + V_{dcx}$	S_1, S_4, S_5, S_8, S_{4k-2}, S_{4k}, S_{4k+1}
10	$V_{dck} - V_{dc2} - V_{dc1}$	S_2, S_3, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+2}
11	$V_{dck} - V_{dc2} - V_{dc1} + V_{dcx}$	S_2, S_3, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+1}
12	$V_{dck} - V_{dc2}$	S_2, S_4, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+2}
13	$V_{dck} - V_{dc2} + V_{dcx}$	S_2, S_4, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+1}
14	$V_{dck} - V_{dc2} + V_{dc1}$	S_1, S_4, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+2}
15	$V_{dck} - V_{dc2} + V_{dc1} + V_{dcx}$	S_1, S_4, S_6, S_7, S_{4k-3}, S_{4k}, S_{4k+1}
16	$V_{dck} - V_{dc1}$	S_2, S_3, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
17	$V_{dck} - V_{dc1} + V_{dcx}$	S_2, S_3, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+1}
18	V_{dck}	S_2, S_4, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
19	$V_{dck} + V_{dcx}$	S_2, S_4, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+1}
20	$V_{dck} + V_{dc1}$	S_1, S_4, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
21	$V_{dck} + V_{dc1} + V_{dcx}$	S_1, S_4, S_6, S_8, S_{4k-3}, S_{4k}, S_{4k+1}
22	$V_{dck} + V_{dc2} - V_{dc1}$	S_2, S_3, S_5, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
23	$V_{dck} + V_{dc2} - V_{dc1} + V_{dcx}$	S_1, S_3, S_5, S_8, S_{4k-3}, S_{4k}, S_{4k+1}
24	$V_{dck} + V_{dc2}$	S_2, S_4, S_5, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
25	$V_{dck} + V_{dc2} + V_{dcx}$	S_2, S_4, S_5, S_8, S_{4k-3}, S_{4k}, S_{4k+1}
26	$V_{dck} + V_{dc2} + V_{dc1}$	S_1, S_4, S_5, S_8, S_{4k-3}, S_{4k}, S_{4k+2}
27	0 V_{dc}	S_1, S_3, S_5, S_7, S_{4k-3}, S_{4k-1}, S_{4k+2}

$$\text{Switch count without DLC circuit} = 4k \tag{2}$$

$$\text{Switch count with DLC circuit} = 4k + 2 \tag{3}$$

3.1 Symmetric MLI

3.1.1 Case 1 (ratio of DC source 1:1:1…): Generally symmetric CHBMLI configuration produces AC voltage waveform with the levels of $2k + 1$. The number of H-bridges to be connected in series depends upon the desired output voltage level. Fig. 1*b* shows CHBMLI configuration with three DC sources and 12 switches. The three DC sources have same voltage magnitude value (1:1:1), so it is called symmetric CHBMLI. The ability of this MLI configuration is to produce seven-level output voltage across the load. The proposed MLI configuration is a combination of CHBMLI with half-bridge inverter circuit as shown in Fig. 1*d*.

The DC source value of CHBMLI without DLC circuit is given below

$$V_{dcj} = V_{dc}, \quad \text{where } j = 1, 2, \ldots, k \tag{4}$$

The DC source value of CHBMLI with DLC circuit is given below

$$\begin{cases} V_{dcj} = V_{dc}, & \text{where } j = 1, 2, \ldots, k \\ V_{dcx} = V_{dc1}/2 \end{cases} \tag{5}$$

A CHBMLI can generate voltage magnitude of V_{dc1}, $V_{dc1} + V_{dc2}$ and $V_{dc1} + V_{dc2} + V_{dc3}$ in each half-cycle across the load. However, the proposed DLC circuit can generate voltage magnitude of V_{dcx}, $V_{dc1} + V_{dcx}$, $V_{dc1} + V_{dc2} + V_{dcx}$ in each half-cycle across the load. The proposed 13-level inverter output voltage magnitude is V_{dcx}, V_{dc1}, $V_{dc1} + V_{dcx}$, $V_{dc1} + V_{dc2}$, $V_{dc1} + V_{dc2} + V_{dcx}$, $V_{dc1} + V_{dc2} + V_{dc3}$ in each half-cycle.

3.2 Asymmetric MLI

Magnitude ratio of DC voltage source can be selected in a way that the numbers of output voltage levels are extended. In this case, the higher number of levels can be generated by a minimum number of DC sources, switches and driver circuits. Magnitude ratio of DC sources will be considered in the following ways: (i) 1:2:3… (natural sequence), (ii) 1:2:4… (binary sequence), (iii) 1:2:6… (quasi-linear sequence) and (iv) 1:3:9… (trinary sequence). The main benefit of using the asymmetric MLI structures is to produce a higher number of levels by eliminating repeated switching combination for a particular voltage level.

3.2.1 Case 2 (ratio of DC source 1:2:3…): The CHBMLI configuration considering natural sequence number of DC source is displayed in Fig. 1*b*. The magnitude of DC sources is in the ratio of 1:2:3…*k*. Generally the ability of this configuration is to produce a voltage level of $k^2 + k + 1$. It can generate a 13-level output voltage with three DC sources and 12 switches.

The DC source value of CHBMLI without DLC circuit is given below

$$V_{dcj} = jV_{dc}, \quad \text{where } j = 1, 2, \ldots k \tag{6}$$

The DC source value of CHBMLI with DLC circuit is given below

$$\begin{cases} V_{dcj} = jV_{dc}, & \text{where } j = 1, 2, \ldots k \\ V_{dcx} = V_{dc1}/2 \end{cases} \tag{7}$$

The proposed DLC circuit is added with the natural sequence of CHBMLI (CHBMLI + DLC), which can generate the 25-level output voltage.

Table 2 Generalised formulas for five different cases of proposed configurations

Case	Name of the DC source sequence	Maximum step of yield voltage	Number of level (N_L)		PIV	
			Without DLC	With DLC	Without DLC	With DLC
1	symmetric sequence $V_{dcj} = V_{dc}$, $V_{dcx} = V_{dc1}/2$, where $j = 1, 2, \ldots, k$	kV_{dc}	$2 \times \left(\sum_{i=1}^{k} 1^i\right) + 1$	$2 \times \left[2 \times \left(\sum_{i=1}^{k} 1^i\right) + 1\right] - 1$	$4\,kV_{dc}$	$(4k+1)V_{dc}$
2	natural sequence $V_{dcj} = jV_{dc}$, $V_{dcx} = V_{dc1}/2$, where $j = 1, 2, \ldots, k$	$\frac{k^2+k}{2}V_{dc}$	$2 \times \left(\sum_{i=1}^{k} i\right) + 1$	$2 \times \left[2 \times \left(\sum_{i=1}^{k} i\right) + 1\right] - 1$	$2k(k+1)V_{dc}$	$\{2k*(k+1)+1\}V_{dc}$
3	binary sequence $V_{dcj} = 2^{j-1}V_{dc}$, $V_{dcx} = V_{dc1}/2$, where $j = 1, 2, \ldots, k$	$(2^k-1)V_{dc}$	$2 \times \left(\sum_{i=0}^{k-1} 2^i\right) + 1$	$2 \times \left[2 \times \left(\sum_{i=0}^{k-1} 2^i\right) + 1\right] - 1$	$4(2^k-1)V_{dc}$	$\{4*(2^k-1)+1\}V_{dc}$
4	quasi-linear sequence $V_{dcj} = \begin{cases} V_{dc} & j = 1 \\ 2 \times 3^{j-2} & j \geq 2 \end{cases}$ where $j = 1, 2, \ldots, k$, $V_{dcx} = V_{dc1}/2$	$\frac{2 \times (3^k-1)}{2}V_{dc}$	$1 + \left(\sum_{k=2}^{\infty} 2 \times 3^{k-1}\right)$	$2 \times \left[1 + \left(\sum_{k=2}^{\infty} 2 \times 3^{k-1}\right)\right] - 1$	$4(3^{k-1})V_{dc}$	$\{4*(3^{k-1})+1\}V_{dc}$
5	trinary sequence $V_{dcj} = 3^{j-1}V_{dc}$, $V_{dcx} = V_{dc1}/2$, where $j = 1, 2, \ldots, k$	$\frac{(3^k-1)}{2}V_{dc}$	$2 \times \left(\sum_{i=0}^{k-1} 3^i\right) + 1$	$2 \times \left[2 \times \left(\sum_{i=0}^{k-1} 3^i\right) + 1\right] - 1$	$2(3^k-1)V_{dc}$	$\{2*(3^k-1)+1\}V_{dc}$

3.2.2 Case 3 (ratio of DC source 1:2:4…): The CHBMLI configuration considering binary sequence number of DC source is displayed in Fig. 1*b*. The voltage magnitude ratio of a binary MLI is 1:2:4…*k*. Generally the binary MLI configuration produces an output voltage level in the form of $2^{k+1}-1$. This MLI configuration can generate up to 15-level output voltage with the help of 12 switches and three DC sources.

The DC source value of CHBMLI without DLC circuit is given below

$$V_{dcj} = 2^{j-1}V_{dc}, \quad \text{where } j = 1, 2, \ldots k \tag{8}$$

The DC source value of CHBMLI with DLC circuit is given below

$$\begin{cases} V_{dcj} = 2^{j-1}V_{dc}, & \text{where } j = 1, 2, \ldots k \\ V_{dcx} = V_{dc1}/2 \end{cases} \tag{9}$$

The proposed DLC circuit is added with binary CHBMLI and can generate up to 29-level output voltage.

3.2.3 Case 4 (ratio of DC source 1:2:6…): Most of the researchers have covered only natural sequence MLI and binary sequence MLI. Apart from these two methods, quasi-linear MLI is one of the best choices to improve the voltage levels and to reduce switching devices. The ratio of DC sources in this MLI configuration is 1:2:6:…*k*. This type of MLI can generate up to 19-level output voltage with the help of 12 switches and three DC sources.

The DC source value of CHBMLI without DLC circuit is given below

$$V_{dcj} = \begin{cases} V_{dc} & \text{for } j = 1 \\ 2 \times 3^{j-2} & \text{for } j \geq 2 \end{cases} \tag{10}$$

The DC source value of CHBMLI with DLC circuit is given below

$$\begin{cases} V_{dcj} = \begin{cases} V_{dc} & \text{for } j = 1 \\ 2 \times 3^{j-2} & \text{for } j \geq 2 \end{cases} \\ V_{dcx} = V_{dc1}/2 \end{cases} \tag{11}$$

The proposed DLC circuit is added with the quasi-linear MLI, which produces up to 37-level output voltage.

3.2.4 Case 5 (ratio of DC source 1:3:9…): In this case, the voltage magnitude of DC sources is considered in the ratio of 1:3:9:…*k* which is called trinary CHBMLI. A CHBMLI configuration considering a trinary sequence number of DC sources is shown in Fig. 1*b*. This configuration can generate up to 27-level output voltage with the help of 12 switches and three DC sources. The concept of trinary DC source CHBMLI is explained in [27].

The DC source value of CHBMLI without DLC circuit is given below

$$V_{dcj} = 3^{j-1}V_{dc}, \quad \text{where } j = 1, 2, \ldots, k \tag{12}$$

The DC source value of CHBMLI with DLC circuit is given below

$$\begin{cases} V_{dcj} = 3^{j-1}V_{dc}, & \text{where } j = 1, 2, \ldots, k \\ V_{dcx} = V_{dc1}/2 \end{cases} \tag{13}$$

The proposed MLI (trinary CHBMLI + DLC) configuration can produce up to 53-level output voltage.

Table 2 shows the comparison for five different cases of CHBMLI without DLC and with DLC configuration with different parameters. The parameter '*k*' represents the number of DC sources in CHBMLI. The calculation of peak inverse voltage (PIV) is used to determine the device ratings. If PIV value is decreased, the total cost of the inverter decreases. For the same number of output level, the proposed configuration requires lesser PIV value when compared with conventional CHBMLI.

4 Modulation technique

According to the switching frequency of MLIs, two major groups can be classified such as fundamental switching frequency and higher switching frequency [5, 28]. In this paper, multicarrier pulse width modulation (PWM) methods are embraced for achieving a better quality of output voltage waveforms. Most of the industries apply sinusoidal PWM (SPWM) technique for creating switching pulses which is the least difficult method. In this method, PWM signals are generated by comparing a sinusoidal signal (reference signal) with triangular carriers (carrier signals). Phase disposition (PD) strategy is employed for the carrier arrangements which has the same peak to peak amplitude and same frequency and is in-phase with each other. This strategy is more suitable for reducing the %THD and distortion factor (DF) when compared with other

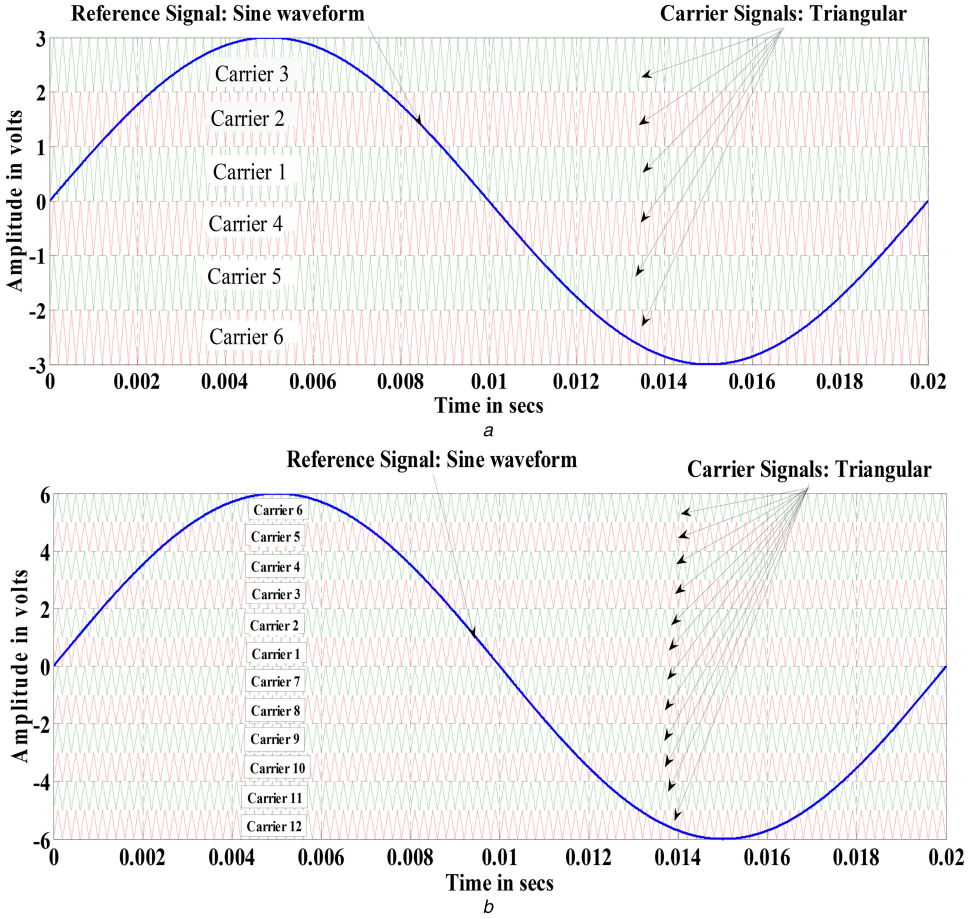

Fig. 2 *SPWM strategy for CHBMLI without and with DLC in case 1*
(a) PD strategy carrier arrangement for seven-level in CHBMLI without DLC, ***(b)*** PD strategy carrier arrangement for 13-level in CHBMLI with DLC

carrier arrangement techniques [29–31]. Figs. 2*a* and *b* show the carrier arrangement for SPWM technique with PD strategy to generate gate pulses of 7-level and 13-level output voltage in symmetric sequence CHBMLI without DLC and with DLC, respectively. From Fig. 2*a*, it can be seen that six carriers are required for generating seven-level output voltage, where carriers are equally arranged above and below the zero reference. The sine reference continuously compared with triangular carriers generates the Boolean outputs. Boolean outputs of each carrier are represented by C_1–C_6. From Fig. 2*b*, it can be seen that 12 carriers are required for generating 13-level output voltage, where carriers are equally arranged above and below the zero reference. Boolean outputs of each carrier are generated by comparing the sine reference with triangular carriers which is represented by C_1–C_{12}. By applying some logical operation with Boolean outputs based on the switching Table 1, the desired PWM pulses are generated for the particular switch which leads to required output voltage level. The simplified logic operation to all switches in CHBMLI without DLC for generating seven-level output voltage is given in (14). The simplified logic operation to all switches in CHBMLI with DLC for generating 13-level output voltage is given in (15)

$$\begin{cases} (S_1, S_8 = C_1), (S_2, S_7 = C_4) \\ (S_3 = C_2), (S_5 = C_3), (S_9 = C_5), (S_{11} = C_6) \\ S_4 = (C_1 * \sim C_2) + (\sim C_1 * C_2) + C_1 \\ S_6 = (C_1 * \sim C_3) + (\sim C_1 * C_3) + C_4 \\ S_{10} = (C_4 * \sim C_5) + (\sim C_4 * C_5) + C_1 \\ S_{12} = (C_4 * \sim C_6) + (\sim C_4 * C_6) + C_4 \end{cases} \tag{14}$$

$$\begin{cases} (S_1 = C_2), (S_3 = C_4), (S_5 = C_6), (S_7 = C_7) \\ (S_8 = C_1), (S_9 = C_9), (S_{11} = C_{11}) \\ S_2 = (C_1 * \sim C_2) + (\sim C_1 * C_2) + C_7 \\ S_4 = (C_1 * \sim C_4) + (\sim C_1 * C_4) + C_1 \\ S_6 = (C_1 * \sim C_6) + (\sim C_1 * C_6) + C_1 \\ S_{10} = (C_7 * \sim C_9) + (\sim C_7 * C_9) + C_7 \\ S_{12} = (C_7 * \sim C_{11}) + (\sim C_7 * C_{11}) + C_1 \\ S_{13} = (C_1 \oplus C_2) + (C_3 \oplus C_4) + (C_5 \oplus C_6) + (C_{11} \oplus C_{12}) \\ S_{14} = (C_2 \oplus C_3) + (C_4 \oplus C_5) + (C_8 \oplus C_9) + (C_{10} \oplus C_{11}) \end{cases} \tag{15}$$

where (+) represents logical operation of OR, (*) represents logical operation of AND, ($\oplus$) represents logical operation of XOR then ($\sim$) represents the logical operation of NOT. The same scenario is followed for generating the PWM pulses of other CHBMLIs and proposed MLIs.

5 Comparative study and parameter analysis

A comparison between the number of DC sources versus number of output voltage level in different cases of CHB without and with DLC configurations are shown in Figs. 3*a* and *b*, respectively. From Figs. 3*a* and *b*, it is clear that the CHBMLI with DLC generates a higher number of output voltage level when compared with CHBMLI without DLC configuration. Where the trinary condition of CHBMLI with DLC configuration generates higher output voltage level compared with other conditions. With increase in number of levels, the utilisation of switches and DC sources will also increase. From the graphical representation in Fig. 3, it can be inferred that the proposed MLI generates a higher number of output voltage level with a minimum number of DC sources.

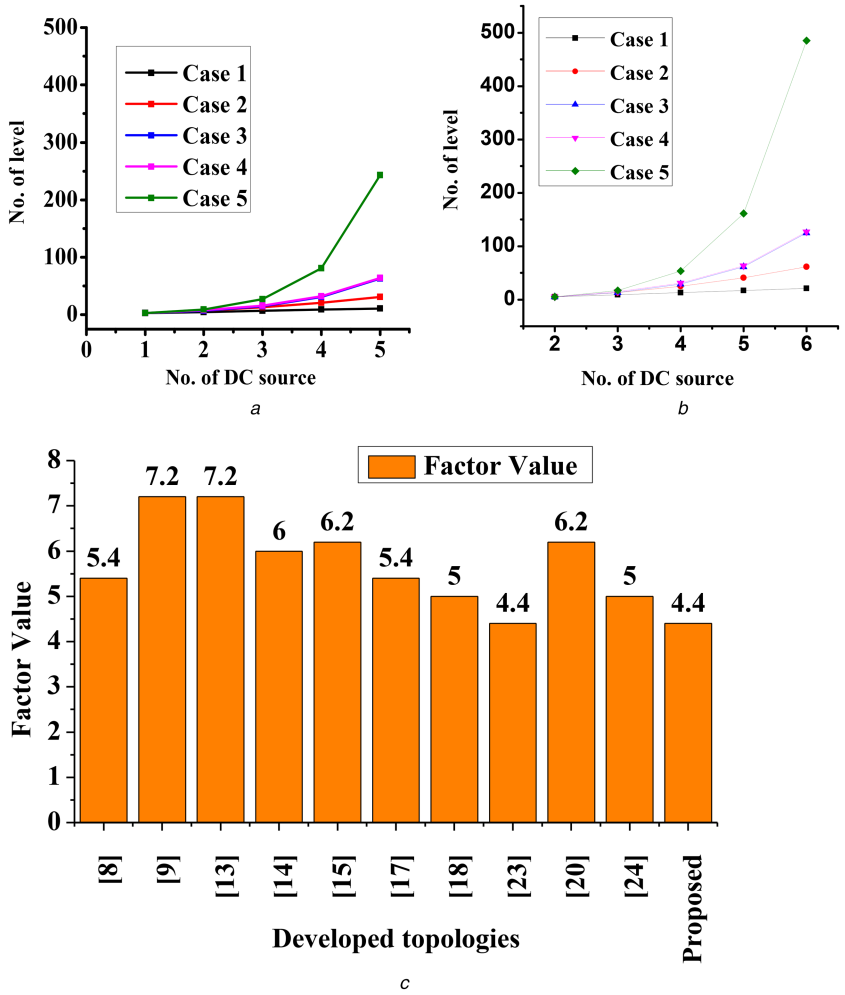

Fig. 3 *Graphical representations*

(a) Number of DC source versus number of level in CHBMLI without DLC, ***(b)*** Number of DC source versus number of level in CHBMLI with DLC (proposed), ***(c)*** Comparison of components per level factor between proposed and other developed topologies

5.1 Calculation of component count using per level factor method

A new method for calculating the components count is called as 'components per level factor' (F_L). The number of poles is the most important parameter to decide the factor value. If the factor value is high, the topology requires more number of components to achieve the desired output voltage level. Hence, the target is to decrease the factor value. This calculation is attempted in [32], but the number of poles (N_P) is not consistent and this may lead to incorrect factor value. Considering this drawback, the number of poles is kept constant for all topologies in this paper for calculating the factor value accurately. Based on three phase configurations, this factor value is determined. The following formula is used to calculate F_L:

$$F_L = \frac{N_S + N_C + N_D + N_{DC} + N_T + N_X}{N_P} \tag{16}$$

where N_S, N_C, N_D, N_{DC}, N_T, N_X and N_P indicate number of switches, number of capacitors, number of diodes, number of source, number of transformers, number of other components and number of voltage level per pole, respectively. A comparison is carried out between the proposed configurations and other topologies presented in the literature for the same number of level (five-level) which is shown in Fig. 3*c*. Table 3 shows the requirement of total components for different topologies to achieve the same voltage level and its corresponding factor value. The topologies utilised in this comparison do not have the number of other components (N_X). In [34], the developed topology has the lowest factor value like proposed topology but the extra circuit is needed for balancing the capacitor. From this comparison, it is more obvious that the proposed configuration requires lesser number of components count.

5.2 Calculation of %THD and distortion factor

Amplitude modulation index plays a vital role in maintaining the desired output voltage waveform. The reduction of modulation index leads to reduced output voltage level and increased %THD. Figs. 4*a* and *b* show the comparison of modulation indices versus %THD in different types of CHBMLI without DLC and with DLC, respectively. From this comparison, it could be confirmed that the proposed trinary CHBMLI has lesser %THD when compared with other configurations. Figs. 4*c* and *d* show the comparison of modulation indices versus DF in different types of CHBMLI without and with DLC, respectively.

5.3 Calculation of power losses

The calculation of power losses is crucial for cost estimation and cooling system designing in MLI. Power losses can be divided into two types such as conduction losses and switching losses. In the low switching frequency, the conduction losses are dominant whereas in high switching frequency the switching losses are considerable. The MLI concept can be extended for any number of levels. Since the number of level is directly proportional to the number of switches. If the switches count increases, the power loss will increase. Therefore, it is proved that the proposed configuration produces lesser power loss when compared with conventional configuration. The study of these losses will also help and enhance the understanding of the characteristics of the proposed MLI topology. Therefore, it becomes essential to

Table 3 Calculation of components per level factor and components count

Developed topologies in	No. of level per pole (N_P)	No. of switches (N_S)	No. of source (N_{DC})	No. of capacitors (N_C)	No. of diodes (N_D)	No. of transformers (N_T)	Components per level factor (F_L)
[8]	5	24	1	2	0	0	5.4
[24]	5	24	6	0	0	0	5
[9]	5	27	9	0	0	0	7.2
[13]	5	15	3	6	12	0	7.2
[14]	5	24	6	0	0	0	6
[15]	5	24	1	6	0	0	6.2
[17]	5	24	1	1	0	1	5.4
[18]	5	18	7	0	0	0	5
[19, 22, 33]	5	18	3	1	0	0	4.4
[20]	5	24	1	6	0	0	6.2
proposed	5	18	4	0	0	0	4.4

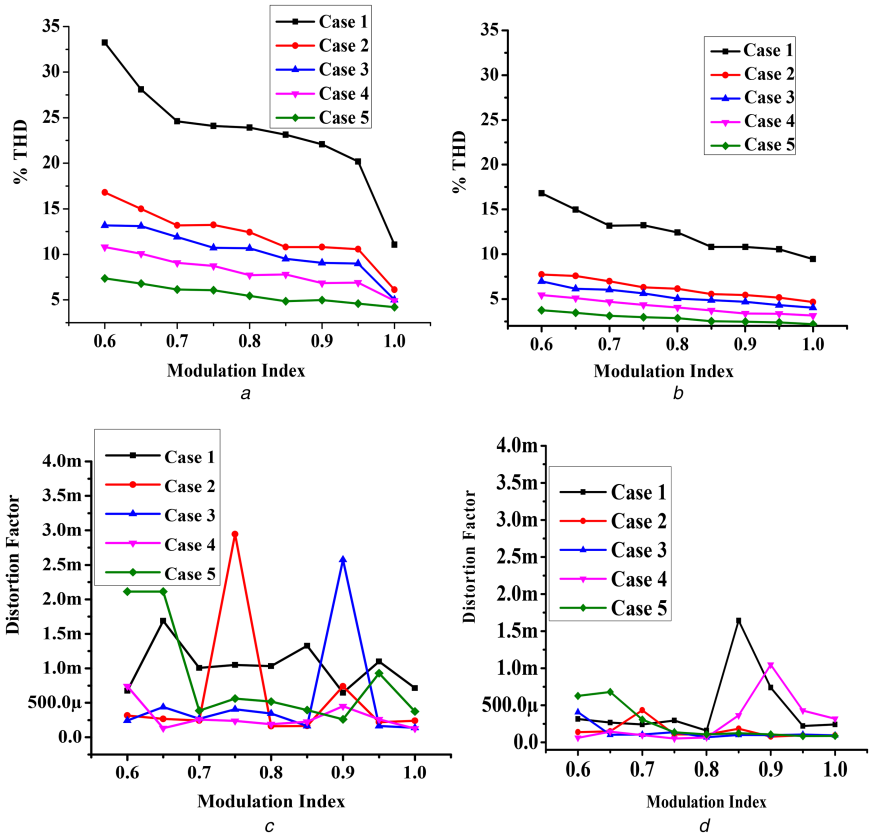

Fig. 4 *Graphical representation for %THD and %DF*

(a) Modulation index versus %THD in CHBMLI without DLC, ***(b)*** Modulation Index versus %THD in CHBMLI with DLC, ***(c)*** Modulation index versus DF in CHBMLI without DLC, ***(d)*** Modulation index versus DF in CHBMLI with DLC

calculate the power losses (switching losses and conduction losses).

Calculation of losses is mandatory to prove the effectiveness of proposed configuration. Conduction loss (P_{cl}) and switching loss (P_{sl}) are the two major types of losses that are related with power electronic switches. The total switching losses (P_l) can be calculated by adding conduction loss and switching loss of each switch which is represented by the following equation:

$$P_l = P_{cl} + P_{sl} \tag{17}$$

5.3.1 Switching losses calculation: The calculation of switching losses is evaluated in a typical switch and is later extended to other switches of proposed MLI [35]. Using linear approximation, the energy loss during turn-on and turn-off period can be calculated [33, 35]. The switching losses can be calculated by multiplying frequency with sum of energy losses in each switch which is represented by the following equation:

$$P_{sl,k} = f \times \sum_{k=1}^{N} \left[\left(E_{off,k} + E_{on,k}\right)\right] \tag{18}$$

During the turn-on period, energy loss can be calculated as follows:

$$E_{off,k} = \int_0^{t_{off}} v(t) \times i(t) \times \mathrm{d}t = \frac{1}{6}\left(v_{sw,k} \times I \times t_{off}\right) \tag{19}$$

During the turn-off period, energy loss can be calculated as follows:

$$E_{on,k} = \int_0^{t_{on}} v(t) \times i(t) \times \mathrm{d}t = \frac{1}{6}\left(v_{sw,k} \times I' \times t_{on}\right) \tag{20}$$

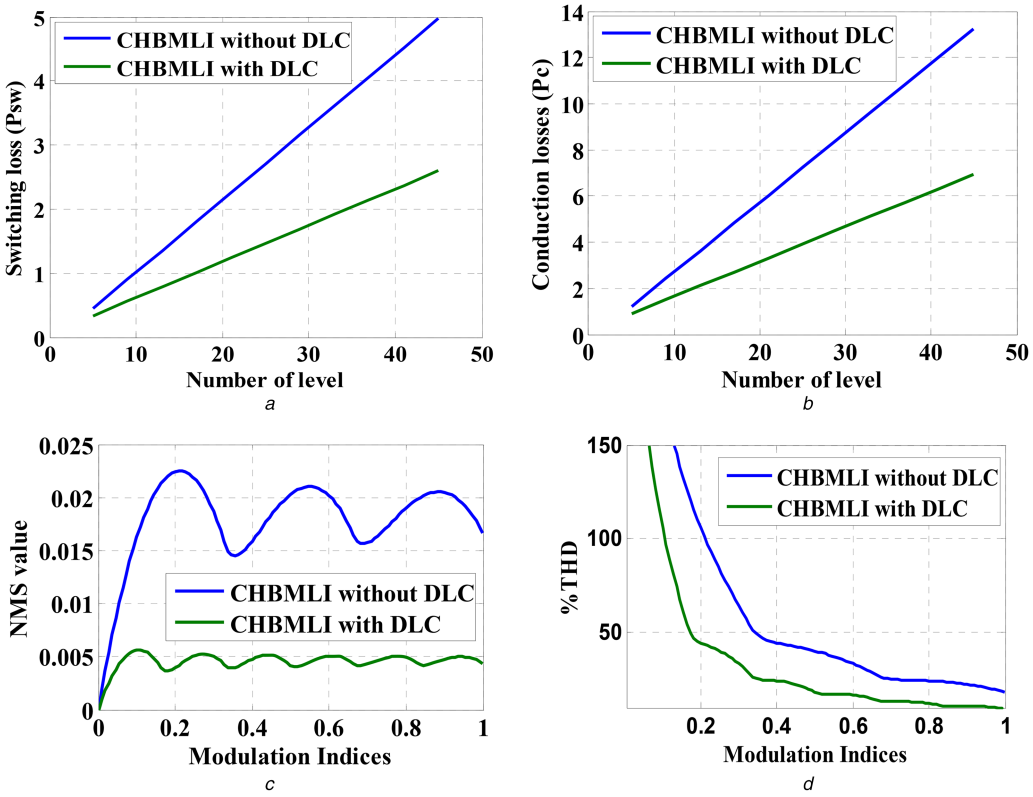

Fig. 5 *Calculation of power loss and theoretical %THD using asymptotic formula*
(a) Switching losses, ***(b)*** Conduction losses, ***(c)*** Voltage ripple NMS value for different modulation indices, ***(d)*** Voltage %THD value for different modulation indices

$E_{\text{off},k}$ represents turn-off energy losses of kth switch, $E_{\text{on},k}$ represents turn-on energy losses of kth switch, t_{off} represents turn-off time of the switch, t_{on} represents turn-on time of the switch, $v_{\text{sw},k}$ represents off-state voltage on the power electronic switch. I' and I represent current through the switch after turning on and before turning off the switch, respectively, f represents the fundamental switching frequency.

5.3.2 Conduction losses calculation: The conduction losses are generated by on-state voltage drop of the switches and equivalent resistance [33]. The conduction losses are evaluated by a typical switch, and then, it is extended to other switches of proposed MLI [33]. Conduction losses exist in switches and also in anti-parallel diode which is represented by the following equation:

$$P_{\text{cl},k} = \sum_{k=1}^{N} \left(P_{\text{cl,t},k} + P_{\text{cl,d},k}\right) \tag{21}$$

The conduction loss in the switch can be calculated as follows:

$$P_{\text{cl,t},k} = \left[\left(V_{\text{t}} \times I_{\text{t,avg}}\right) + \left(r_{\text{t}} \times I_{\text{t,rms}}^2\right)\right] \tag{22}$$

The conduction loss in the anti-parallel diode can be calculated as follows:

$$P_{\text{cl,d},k} = \left[\left(V_{\text{d}} \times I_{\text{d,avg}}\right) + \left(r_{\text{d}} \times I_{\text{d,rms}}^2\right)\right] \tag{23}$$

Here, $P_{\text{cl,t},k}$ represents conduction losses in kth switch, $P_{\text{cl,d},k}$ represents conduction losses in kth anti-parallel diode, V_{t} and V_{d} represent on-state voltage of the switch and diode, respectively, r_{t} and r_{d} represent collector emitter on-state resistance of switch, and diode on-state resistance, respectively, $I_{\text{t,avg}}$ and $I_{\text{t,rms}}$ represents average switch current and root-mean-square (RMS) switch current, $I_{\text{d,avg}}$ and $I_{\text{d,rms}}$ represent diode average current and diode RMS current, respectively. Figs. 5*a* and *b* show the comparison of switching losses and conduction losses for CHBMLI without DLC circuit and with DLC circuit in different voltage levels. For simplicity, case 1 only considered for plotting the graph. From that graph, it is clearly understood that the CHBMLI with DLC circuit provides lower switching and conduction losses when compared with CHBMLI without DLC circuit.

5.4 Theoretical calculation of %THD

Most of the research papers are ended with the simulated %THD. However, in this paper the %THD value is calculated in theoretical and also in simulation. THD is easily calculated in time domain using voltage ripple normalised mean square (NMS) criterion [36, 37]. The general formula for calculating the NMS and THD is represented by (24) and (25), respectively

$$\text{THD} = \frac{\sqrt{2} \times \sqrt{\text{NMS}}}{m} \times 100\% \tag{24}$$

(see (25)) The above NMS equation can be extended to any number of voltage levels. The voltage ripple NMS value purely

$$\begin{aligned}\text{NMS},(m) = \Bigg\{ & \frac{2}{\pi \times [n-1]} \times m - \left(0.5 \times m^2\right), \quad 0 \le m < \frac{1}{n-1} \\ & \frac{2}{\pi \times [n-1]} \times m - \left(0.5 \times m^2\right) - \frac{k \times [k+1]}{[n-1]^2} + \frac{4}{\pi \times [n-1]^2} \times \sum_{i=1}^{k} i \times \arcsin\left(\frac{i}{[n-1] \times m}\right) \\ & + \frac{4}{\pi \times [n-1]} \times \sum_{i=1}^{k} \sqrt{m^2 - \frac{i^2}{[n-1]^2}}, \quad \frac{k}{n-1} \le m < \frac{k+1}{n-1}, \quad 1 \le k \le n-2 \Bigg\}\end{aligned} \tag{25}$$

depends on the modulation index. Figs. 5*c* and *d* show the value of voltage ripple NMS for different modulation indices and theoretical %THD value for different modulation indices, respectively, in CHBMLI without DLC and with DLC. For simplicity, only case 1 is considered for plotting the graph. From these graphs it is clearly shown that %THD is lesser in CHBMLI with DLC configuration when compared with without DLC configuration. Table 4 shows the comparison of proposed topology with conventional MLI topologies. From Table 4, the proposed topology requires fewer components for generating higher number of output voltage level. Also, the conduction of switches per voltage level and the PIV is lower compared with other topologies which reduce the cost and losses.

6 Simulation and experimental results

A symmetric CHBMLI and four different cases of asymmetric CHBMLI (natural sequence, binary sequence, quasi-linear sequence and trinary sequence) are tested with simulation and experimental setup under two conditions: (i) CHBMLI without integrated DLC circuit and (ii) CHBMLI with integrated DLC circuit. Experimental setup of the proposed MLI configuration incorporates four DC sources, FGA25N120 insulated-gate bipolar transistor as switching devices, driver circuit with TLP250, measurement devices (voltage differential probe, current probe and mixed signal oscilloscope), dSpace controller (1104) and a resistive inductive (*RL*) load of 100 Ω and 20 mH. The switching frequency is 5 kHz.

6.1 CHBMLI without integrated DLC circuit

The symmetric CHBMLI configuration can generate seven-level output voltage waveform with 12 switches. The three DC sources have same values $V_{dc1} = V_{dc2} = V_{dc3} = 20$ V. The gating signal of the switches is generated by multicarrier based SPWM in PD method which is described in Section 4. Fig. 6*a* demonstrates the experimental seven-level output voltage waveform of symmetric CHBMLI. Fig. 6*b* shows the experimental 13-level output voltage waveform of natural sequence CHBMLI configuration. The DC voltage source values are chosen in the ratio of 1:2:3 such as $V_{dc1} = 20$ V, $V_{dc2} = 40$ V, $V_{dc3} = 60$ V. The 15-level experimental output voltage waveform of binary sequence CHBMLI configuration is shown in Fig. 6*c*, where the voltage source values are different such as $V_{dc1} = 20$ V, $V_{dc2} = 40$ V, $V_{dc3} = 80$ V. The DC voltage source ratio of quasi-CHBMLI and trinary CHBMLI configurations are 1:2:6 and 1:3:9, respectively. The value of DC sources in quasi-MLI and trinary MLI configurations are $V_{dc1} = 20$ V, $V_{dc2} = 40$ V, $V_{dc3} = 120$ V and $V_{dc1} = 20$ V, $V_{dc2} = 60$ V, $V_{dc3} = 180$ V, respectively. Fig. 6*d*. shows the experimental output voltage waveform of quasi-linear MLI and trinary MLI which generates 19-level and 27-level, respectively.

Table 4 Comparison of proposed topology with conventional topologies

Parameters	DCMLI	FCMLI	CHBMLI	Proposed MLI
no. of level	13	13	13	13
no. of diodes	132	—	—	—
no. of capacitors	—	66	—	—
no. of DC bus capacitor	12	12	—	—
no. of switches	24	24	24	14
no. of DC sources	1	1	6	4
no. of driver circuits	24	24	24	14
conducting switches per voltage level	12	12	12	7
total PIV	24 V_{dc}	24 V_{dc}	24 V_{dc}	13 V_{dc}
total components count	193	127	54	32

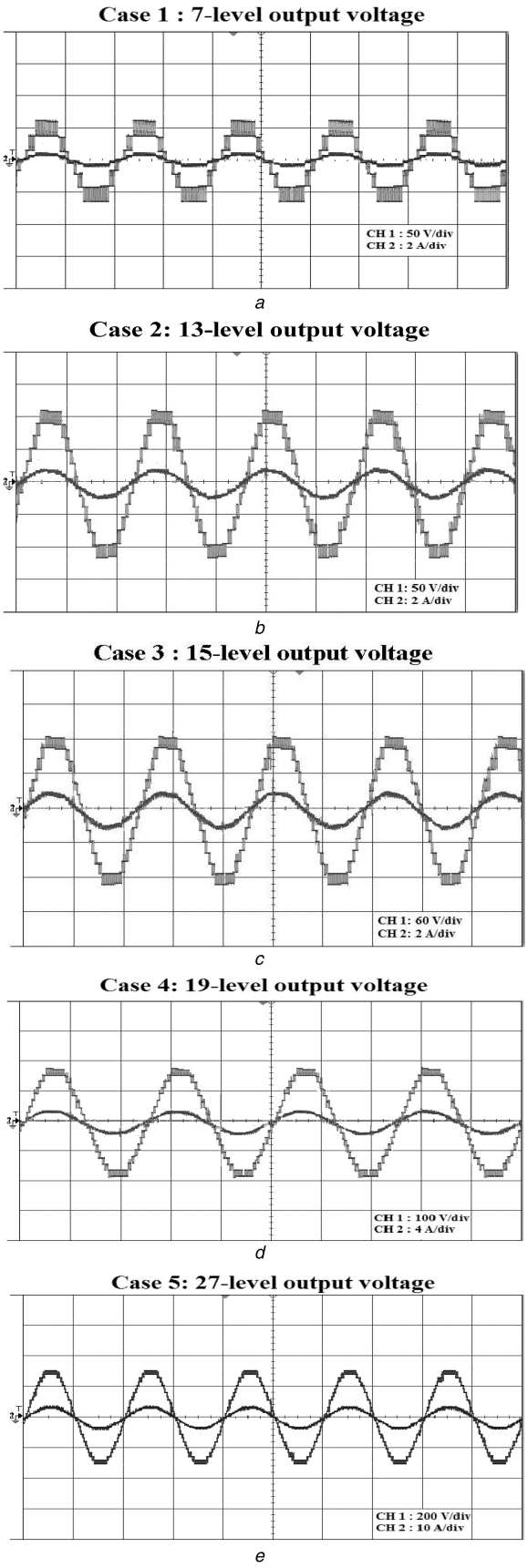

Fig. 6 *Experimental output voltage waveforms for CHB without DLC configurations*

(a) Case 1: seven-level output voltage for symmetric sequence, ***(b)*** Case 2: 13-level output voltage for natural sequence, ***(c)*** Case 3: 15-level output voltage for binary sequence, ***(d)*** Case 4: 19-level output voltage for quasi-linear sequence and case 5: 27-level output voltage for trinary sequence

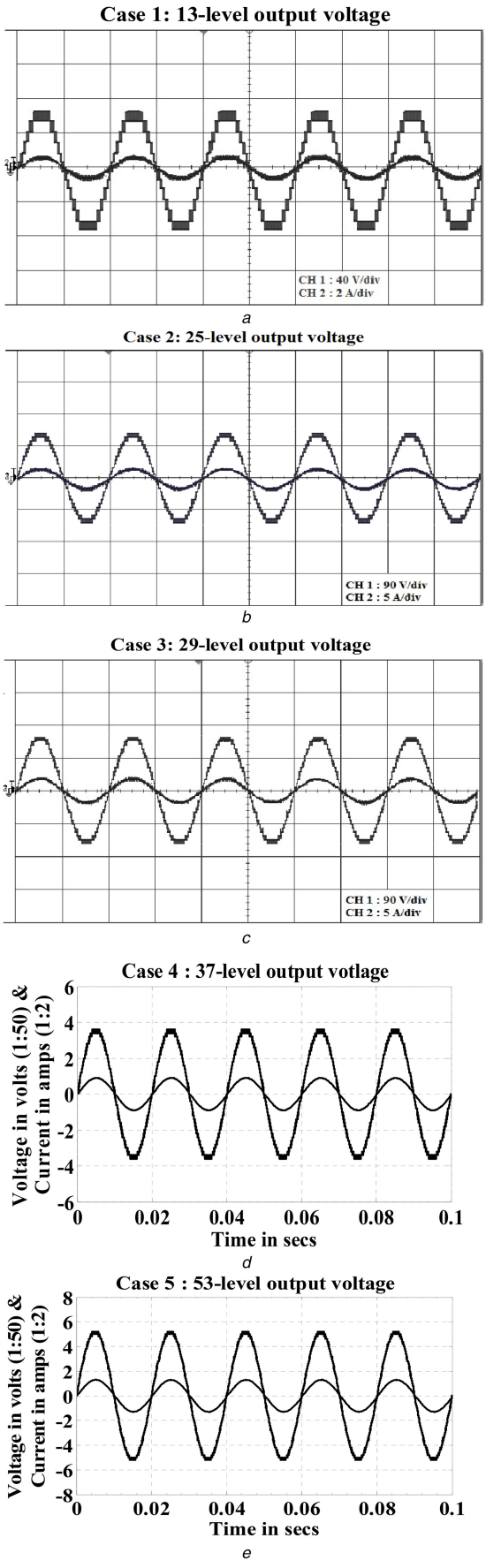

Fig. 7 *Experimental (cases 1–3) and simulation (cases 4 and 5) output voltage waveforms for CHB with DLC configurations*

(a) Case 1: 13-level output voltage, ***(b)*** Case 2: 25-level output voltage, ***(c)*** Case 3: 29-level output voltage, ***(d)*** Case 4: 37-level output voltage and case 5: 53-level output voltage

6.2 CHBMLI with integrated DLC circuit

The performance of proposed (CHB with DLC) configuration is validated experimentally. The value of first DC source for proposed configurations is $V_{dc1} = 20$ V for all cases in simulation and experiment. The voltage source value of DLC circuit is $V_{dcx} = 0.5*V_{dc1} = 10$ V for all cases. The proposed symmetric CHBMLI is capable of generating up to 13-level output voltage waveform. Fig. 7*a*. shows the 13-level experimental output voltage with steps of 10 V each and THD of 9.46%. The DLC circuit is added with natural sequence of CHBMLI configuration which is used to generate a 25-level experimental output voltage waveform which is shown in Fig. 7*b*. Fig. 7*c* shows the 29-level experimental output voltage waveform of proposed binary sequence CHBMLI. Fig. 7*d* represents the simulation output voltage waveforms of 37-level and 53-level in proposed quasi-linear and trinary sequence CHBMLI, respectively.

7 Conclusion

A new configuration of MLI (CHB + DLC) has been introduced in this paper, which delivers nearly twice the actual output voltage level. Many configurations have utilised higher magnitude of DC values to increase the output voltage level. However, in this paper the lower magnitude of DC value is considered for DLC such as $V_{dcx} = 0.5*V_{dc1}$ to reduce the PIV. For case 1, the proposed configuration has PIV of $13*V_{dc}$ whereas the conventional topologies requires $24*V_{dc}$. Also, the proposed configuration requires 7 conducting switches per voltage level whereas in conventional topologies requires 12 switches for generating the same output voltage level. The working principle of proposed configuration and the mathematical expressions corresponding to output voltage level, maximum possible step, PIV and a plan of action to choose the DC sources have been included in this work. Multicarrier SPWM technique has been presented with logical expressions for generating gating signals. The comparison between five different configurations of CHBMLI with and without DLC configurations including the factors such as the %THD and DF has been exhibited along with experimental results. A new method for calculating the total component count has been described. The proposed configuration has minimum component per level factor and the value is 4.4. The calculation of power losses and theoretical calculation of %THD has been explained with the mathematical formula. The CHBMLI with DLC configurations have lesser power loss and %THD value, when compared with CHBMLI without DLC configurations. From simulation and experimental results and their comparisons, it could be indicated that the proposed configurations provide a better quality output voltage waveform when compared with conventional configurations.

8 References

[1] Lai, J., Peng, F.Z.: 'Multilevel converters – a new breed of power converters', *IEEE Trans. Ind. Appl.*, 1996, **32**, (3), pp. 509–517

[2] Tolbert, L.M., Peng, F.Z.: 'Multilevel converters for large electric drives', *IEEE Trans. Ind. Appl.*, 1999, **35**, (1), pp. 36–44

[3] Rodríguez, J., Lai, J.: 'Multilevel inverters: a survey of topologies, controls applications', *IEEE Trans. Ind. Electron.*, 2002, **49**, (4), pp. 724–738

[4] Rodriguez, J., Bernet, S., Steimer, P.K., *et al.*: 'A survey on neutral-point-clamped inverters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2219–2230

[5] Colak, I., Kabalci, E., Bayindir, R.: 'Review of multilevel voltage source inverter topologies and control schemes', *Energy Convers. Manage.*, 2011, **52**, (2), pp. 1114–1128

[6] Malinowski, M., Rodriguez, J., Pérez, M.A.: 'A survey on cascaded multilevel inverters', *IEEE Trans. Ind. Electron.*, 2010, **57**, (7), pp. 2197–2206

[7] Liu, Y., Luo, F.L.: 'Multilevel inverter with the ability of self-voltage balancing', *IEE Proc., Electr. Power Appl.*, 2006, **153**, (1), pp. 105–115

[8] Thathan, M., Alexander, A.: 'Modelling and analysis of modular multilevel converter for solar photovoltaic applications to improve power quality', *IET Renew. Power Gener.*, 2015, **9**, (1), pp. 78–88

[9] Jiang, F., Tu, C., Shuai, Z., *et al.*: 'Multilevel cascaded-type dynamic voltage restorer with fault current-limiting function', *IEEE Trans. Power Deliv.*, 2016, **31**, (3), pp. 1261–1269

[10] Leo, J.D., Escalante, M.F., Mata-Jimenez, M.T.: 'Observer for dc voltages in a cascaded H-bridge multilevel STATCOM', *IET Electr. Power Appl.*, 2007, **1**, (6), pp. 879–889

[11] Rini Ann Jerin, A., Palanisamy, K., Umashankar, S., *et al.*: 'Power quality improvement of grid connected wind farms through voltage restoration using dynamic voltage restorer', *Int. J. Renew. Energy Res.*, 2016, **6**, (1), pp. 1316–1323
[12] Lin, B.R., Huang, C.H.: 'Analysis and implementation of a single-phase capacitor-clamped inverter with simple structure', *IEEE Proc., Electr. Power Appl.*, 2004, **151**, (5), pp. 555–562
[13] Babaei, E., Moeinian, M.S.: 'Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem', *Energy Convers. Manage.*, 2010, **51**, (11), pp. 2272–2278
[14] Babaei, E., Laali, S., Bayat, Z.: 'A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches', *IEEE Trans. Ind. Electron.*, 2015, **62**, (2), pp. 922–929
[15] Babaei, E., Alilu, S., Laali, S.: 'A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge', *IEEE Trans. Ind. Electron.*, 2014, **61**, (8), pp. 3932–3939
[16] Babaei, E., Laali, S., Alilu, S.: 'Cascaded multilevel inverter with series connection of novel H-bridge basic units', *IEEE Trans Ind. Electron.*, 2014, **61**, (12), pp. 6664–6671
[17] Rahim, N.A., Fathi, M.E.M., Hew, W.P.: 'Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing', *IEEE Trans. Ind. Electron.*, 2013, **60**, (8), pp. 2943–2956
[18] Khosroshahi, M.T.: 'Crisscross cascade multilevel inverter with reduction in number of components', *IET Power Electron.*, 2014, **7**, (12), pp. 2914–2924
[19] Kumar, P.R., Karthik, R.S., Gopakumar, K., *et al.*: 'Seventeen-level inverter formed by cascading flying capacitor and floating capacitor H-bridges', *IEEE Trans. Power Electron.*, 2015, **30**, (7), pp. 3471–3478
[20] Cipriano, E., Helder, J., Muniz, G., *et al.*: 'Nested multilevel topologies', *IEEE Trans. Power Electron.*, 2015, **30**, (8), pp. 4058–4068
[21] Panda, A.K., Suresh, Y.: 'Performance of cascaded multilevel inverter by employing single and three-phase transformers', *IET Power Electron.*, 2012, **5**, (9), pp. 1694–1705
[22] Rech, C., Pinheiro, J.R.: 'Hybrid multilevel converters: unified analysis and design considerations', *IEEE Trans. Ind. Electron.*, 2007, **54**, (2), pp. 1092–1104
[23] Odeh, C.I.: 'A single-phase hybrid multilevel inverter', *Electric Power Compon. Syst.*, 2015, **43**, (3), pp. 252–259
[24] Batschauer, A.L., Mussa, S.A., Heldwein, M.L.: 'Three-phase hybrid multilevel inverter based on half-bridge modules', *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 668–678
[25] Mariethoz, S.: 'Systematic design of high-performance hybrid cascaded multilevel inverters with active voltage balance and minimum switching losses', *IEEE Trans. Power Electron.*, 2013, **78**, (7), pp. 3100–3113
[26] Mariethoz, S.: 'Design and control of high performance modular hybrid asymmetrical cascade multilevel inverters', *IEEE Trans. Ind. Appl.*, 2014, **50**, (6), pp. 4018–4027
[27] Rodríguez, J., Bernet, S., Wu, B., *et al.*: 'Multilevel voltage-source-converter topologies for industrial medium-voltage drives', *IEEE Trans. Ind. Electron.*, 2007, **54**, (6), pp. 2930–2945
[28] Palanivel, P., Dash, S.S.: 'Analysis of THD and output voltage performance for cascaded multilevel inverter using carrier pulse width modulation techniques', *IET Power Electron.*, 2011, **4**, (8), pp. 951–958
[29] Prabaharan, N., Palanisamy, K.: 'Comparative analysis of symmetric and asymmetric reduced switch MLI topologies using unipolar pulse width modulation strategies', *IET Power Electron.*, 2016, **9**, (15), pp. 2808–2823
[30] Prabaharan, N., Palanisamy, K.: 'Analysis and integration of multilevel inverter configuration with boost converters in a photovoltaic system', *Energy Convers. Manage.*, 2016, **128**, pp. 327–342
[31] Luukko, V.N.J., Pyrho, T.I.O., Pyrho, J.: 'Modulation technique for series-connected H-bridge multilevel converters with equal load sharing', *IET Power Electron.*, 2009, **2**, (3), pp. 275–286
[32] Salem, A., Ahmed, E.M., Orabi, M., *et al.*: 'New three-phase symmetrical multilevel voltage source inverter', *IEEE J. Emerg. Sel.Top. Circuits Syst.*, 2015, **5**, (3), pp. 430–442
[33] Kangarlu, M.F., Babaei, E.: 'A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters', *IEEE Trans. Power Electron.*, 2013, **28**, (2), pp. 625–636
[34] Chattopadhyay, S.K., Chakraborty, C.: 'A new multilevel inverter topology with self-balancing level doubling network', *IEEE Trans. Ind. Electron.*, 2014, **61**, (9), pp. 4622–4631
[35] Ebrahimi, J., Babaei, E., Gharehpetian, G.B.: 'A new multilevel converter topology with reduced number of power electronic components', *IEEE Trans. Ind. Electron.*, 2012, **59**, (2), pp. 655–667
[36] Ruderman, A., Reznikov, B., Busquets-Monge, S.: 'Asymptotic time domain evaluation of a multilevel multiphase PWM converter voltage quality', *IEEE Trans. Ind. Electron.*, 2013, **60**, (5), pp. 1999–2009
[37] Ruderman, A.: 'About voltage total harmonic distortion for single-and three-phase multilevel inverters', *IEEE Trans. Ind. Electron.*, 2015, **62**, (3), pp. 1548–1551